Simplified DAC / ADC Lecture Notes

This is a tutorial project to illustrate simplified operation of a Digital to Analog Converter (DAC), and an Analog to Digital Converter (ADC).

Weighted Resistor Digital to Analog Converter

A schematic diagram of a weighted summing amplifier is drawn to the right. A switch connects an input either to a common voltage \( V \) or to a common ground. Only switches currently connected to the voltage source contribute current to the non-inverting input summing node.

The output voltage is given by the expression drawn below the circuit diagram; \( S_X = 1 \) if switch \( X \) connects to \( V \), \( S_X = 0 \) if it connects to ground. There are eight possible combinations of connections for the three switches, and these are indicated in the columns of the table to the right of the diagram. Each combination is associated with a decimal integer as shown. The inputs are weighted in a 4:2:1 relationship, so that the sequence of values for \( 4S_3 + 2S_2 + S_1 \) form a binary-coded decimal number representation. The magnitude of \( V_0 \) varies in units (steps) of \( (R_f/4R)V \) from 0 to 7. This circuit provides a simplified Digital to Analog Converter (DAC). The digital input controls the switches, and the amplifier provides the analog output.

Simplified PSpice Simulation

An illustrative circuit design is shown to the right, with the switch arrangements replaced by three square-wave voltage sources used to produce the eight possible binary input voltage combinations.

A simplified circuit implemented in PSpice is shown to the left. Pulse square-wave voltage sources are used to provide the respective resistor inputs.

Various voltages are plotted below to illustrate circuit behavior. The ‘binary’ input voltages are drawn with an offset voltage is added to clarify the drawings. The DAC output is shown in the following plot. Note: the source voltages are defined negative arbitrarily, simply to obtain a positive DAC output after inversion.
Alternative DAC Implementation
An alternative DAC illustration (Schematics) is drawn below. V0, V1, and V4 are square-wave pulse sources with periods of 0.5ms, 1.0ms, and 2.0 ms respectively. The voltage-controlled switch pairs are operated so that when one switch is opened the other is closed, and vice-versa. A switch pair thus either connects Vref (=1v) to a weighted-resistor input, or the connection is to ground. (Incidentally open- and closed switch resistances are set to 1 megohm and 1 ohm respectively.)

The DAC output is plotted below, as well as the several summing input voltages.
R-2R Ladder DAC
The upper circuit in the figure to the right illustrates a section of a periodic network; the input resistance of the section is R. The second network cascades a second section onto the first, replacing the 2r termination resistor. Finally a third section is added to provide a three-bit binary current division. (Additional sections not used for this illustration can be added.)

In the circuit below a three-section R-2R ladder is connected to a switch network so that either a fixed voltage V is applied to each section as shown, or a ground connection is made. The current contribution through each switch (apply superposition) is as noted; Sx is a binary variable which has the value 1 is the voltage connection is made, and the value 0 for a ground connection.

The current from the ladder is fed to an inverting amplifier, and the output voltage Vo is

\[ \varepsilon_0 = -R_f \left( S_3 \frac{V}{2R} + S_2 \frac{V}{4R} + S_1 \frac{V}{8R} \right) = -R_f \frac{V}{24R} \left( 4S_3 + 2S_2 + S_1 \right) \]
**PSpice Simulation**

Waveforms for a PSpice simulation of a 3-bit R-2R ladder DAC using square-wave pulse voltage sources in place of switches are drawn below; the Schematics diagram for the circuit follows.

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**Current-Switched R-2R DAC**

In general switching a voltage is not favored because inevitable circuit capacitance tends to slow the switching; it is preferable to switch currents since circuit inductances are less troublesome. An illustrative current-switched R-2R DAC circuit diagram is drawn below.

A JFET is used to provide switching operations in conjunction with fixed current sources driving the R-2R ladder. When the JFET is cutoff the current source is connected into the ladder. For a zero gate-source voltage the JFET forms a low-resistance bypass around the current source.
DAC voltages are illustrated next.
Simplified Analog to Digital Converter (ADC)

There are several methods for ADC operation; ‘counting’, SAR comparison, dual ramp, flash, and tracking.

A ‘counting’ converter, whose simplicity is offset by relative slowness, simply compares the output of a DAC to the unknown analog input; when the DAC output first exceeds the analog input the conversion cycle is stopped and the DAC digital input at that time provides the ADC output.

‘Unknown’ input voltages of 2.5v and 6.5v respectively are input; see V(V8) below.

The amplifier switches its output saturation state when the DAC voltage exceeds the ‘unknown’ voltage. Note that this means a finite voltage resolution.
**Successive Approximation Register (SAR) ADC**

The conversion time of the ‘counting’ converter must allow for the possibility that the maximum rated analog input voltage is applied, allow for a comparison at each step. The SAR ADC, while it operates in a similar manner, uses a much more efficient search process.

Consider a three-bit conversion for simplicity. The counting ADC must allow for up to eight comparisons (including zero). The search tree for an SAR search is illustrated to the right. To start a conversion cycle a three-bit digital register is first cleared, and then loaded with the triplet 100. The register state provides the input to a DAC, and that provides a reference output. This output is compared to the analog signal to be converted, and a decision is made whether the analog signal is greater than or less than the reference signal.

This comparison is essentially the same as that made for the ‘counting’ ADC, except that because of the use of the ‘half-way’ code the result of this single comparison is used to eliminate concurrently half the possible DAC steps. As the tree suggests, if the analog signal is greater then all the smaller DAC outputs are eliminated from consideration.

Digital logic associated with the comparison then either clears the MSB (Most Significant Bit) to 0 or simply leaves it unchanged. In either case the next bit is set to 1, i.e., to the mid-code of the selected half, and a new comparison made. Again half the remaining DAC states are eliminated from consideration. Depending on the result of the comparison the second bit is cleared to 0, or it is left unchanged at 1.

In either case the third bit is set to 1 and the comparison step repeated. Each time a comparison is made half the remaining DAC output states will be eliminated. Instead of having to step through \(2^N\) states for an N bit conversion only N comparisons are needed. The SAR ADC is perhaps the most common of the converters, providing a relatively rapid and relatively inexpensive conversion.

**‘Flash’ Converter**

Making all the comparisons between the digital states and the analog signal concurrently makes for a fast conversion cycle. A resistive voltage divider (see figure) can provide all the digital reference states required. There are eight reference values (including zero) for the three-bit converter illustrated. Note that the voltage reference states are offset so that they are midway between reference step values.

The analog signal is compared concurrently with each reference state; therefore a separate comparator is required for each comparison. Digital logic then combines the several comparator outputs to determine the appropriate binary code to present.
A PSpice circuit configuration for a flash converter is illustrated below. (The evaluation version of PSpice sets various limits on the number of components that can be modeled. To simplify the circuit (while retaining the essential concepts) the comparator is replaced by a voltage-controlled switch (Sbreak) set to close when the unknown voltage (‘ana’ for analog) exceeds the reference voltage from the resistive divider network by 0.1 volt, and open when the difference is less than zero. The ‘ON’ resistance of the switch is set to 1 Ω, and the OFF resistance is 1 MegΩ. The ‘comparator’ output voltage is essentially zero when the switch is open and is 5v (chosen more or less arbitrarily as a representative logic voltage) when it is closed. The reference voltages are set to 0.5, 1.5, 2.5, 3.5, 4.5, 5.5, 6.5, and 7.5 volts respectively. The comparator outputs are labeled correspondingly as 1, 2, 3, 4, 5, 6, and 7 respectively. Note that if the unknown input voltage exceeds the voltage of level n then output n and all lower outputs are at 5 v.

Digital logic to convert the ‘comparator’ outputs to appropriate bit values is drawn below the comparator circuit; inputs to the logic are the comparator outputs. The most significant bit B2 is 1 if output 4 is at 5 volts; this implies one of outputs 7, 6, 5, or 4 is at 5 volts. The next significant bit B1 is 1 if either 7 or 6 is ‘high’, or if 4 is ‘low’ (MSB is 0) and concurrently 3 or 2 is ‘high’. The limited availability of parts in the evaluation version requires the use of a NOR gate and an inverter for the output.

The least significant bit is 1 if 7 is high or if 5 is high but not 6 or 7). In addition the LSB is 1 if 4 is low, 3 is high, or if 4 and 2 both are low and 1 is high. Implementing this logic in spite of the limits of the evaluation version involved some modest contortions.
The circuit as drawn is larger than the evaluation version of PSpice will allow. To bypass this constraint the digital computation is done in two parts. In the one case B2 and B1 are computed, and in the other B2 and B0 are computed. The two results are combined in a ‘paint’ program as drawn below. The analog input voltage V(ana) provided by the pulse source is set for pulse amplitudes of 2 (010) and 5 (101) volts respectively.